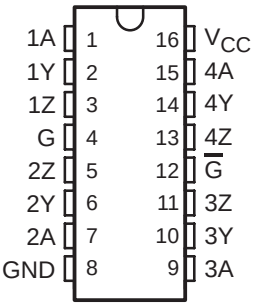
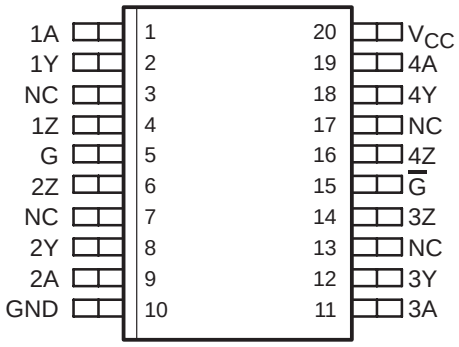
- **Meets or Exceeds EIA Standard RS-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Support Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75172**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC − No internal connection

description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

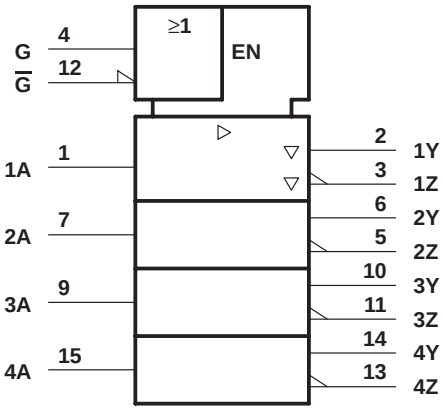
The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of −40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

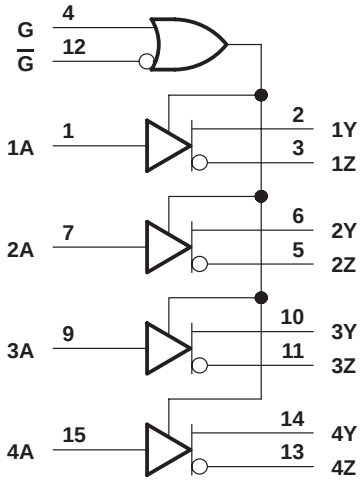
H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic symbol†

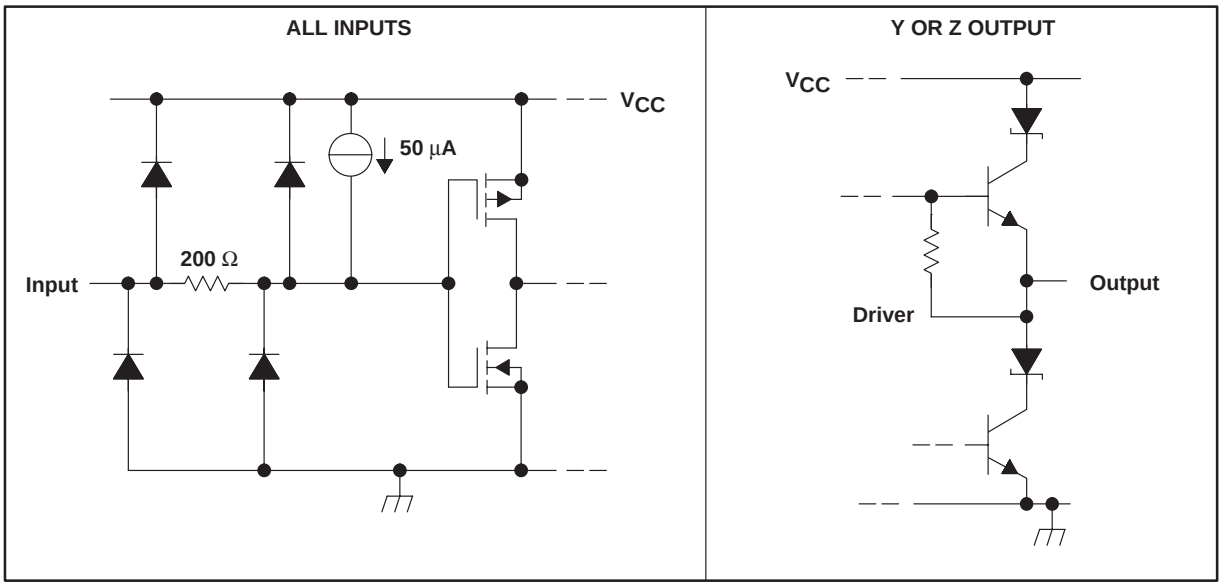


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Output voltage range, V_O . . . . . −10 V to 15 V
Voltage range at A, $\overline{G}$, G . . . . . −0.3 V to V_{CC} + 0.5 V
Continuous power dissipation . . . . . Internally limited‡
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				−7	
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A	SN65LBC172	−40		85	°C
	SN75LBC172	0		70	

DISSIPATION RATING TABLE

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DW	Low K†	1094 mW	10.4 mW/°C	625 mW	469 mW
	High K‡	1669 mW	15.9 mW/°C	954 mW	715 mW
N		1150 mW	9.2 mW/°C	736 mW	598 mW

† In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
‡ In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\|V_{OD}\|$	Differential output voltage‡	R_L = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R_L = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = − 7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = − 7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			10	15	25	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		20	30	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		21	30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		48	70	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		21	30	ns

PARAMETER MEASUREMENT INFORMATION

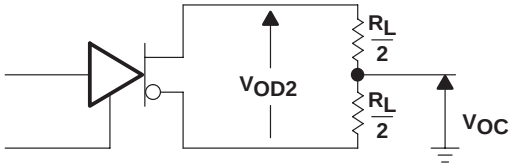
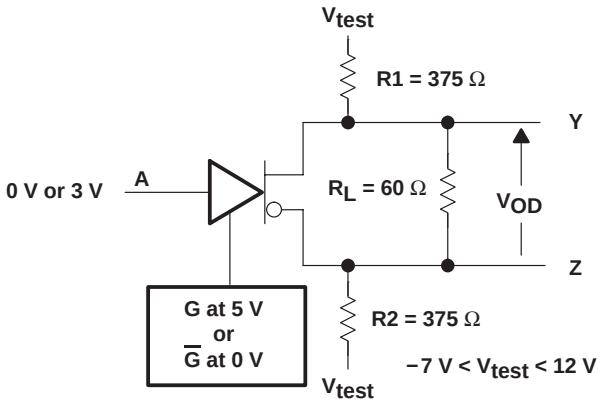
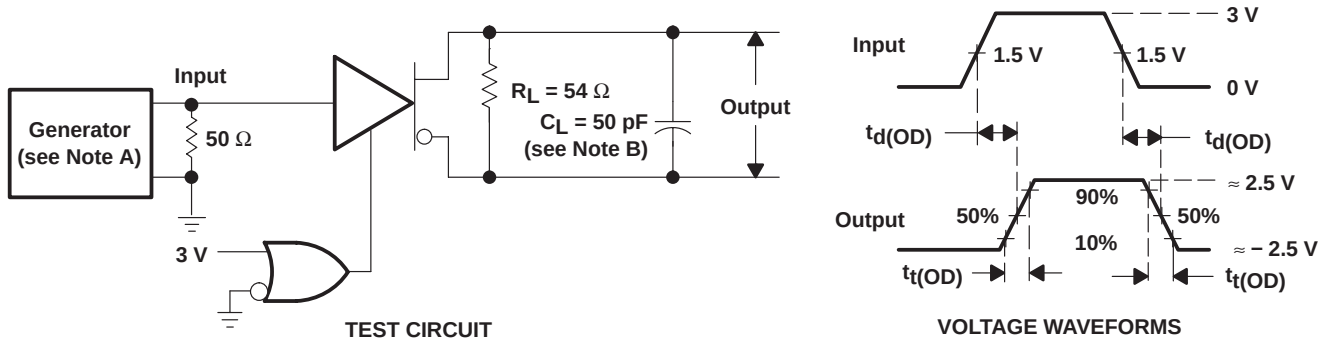


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

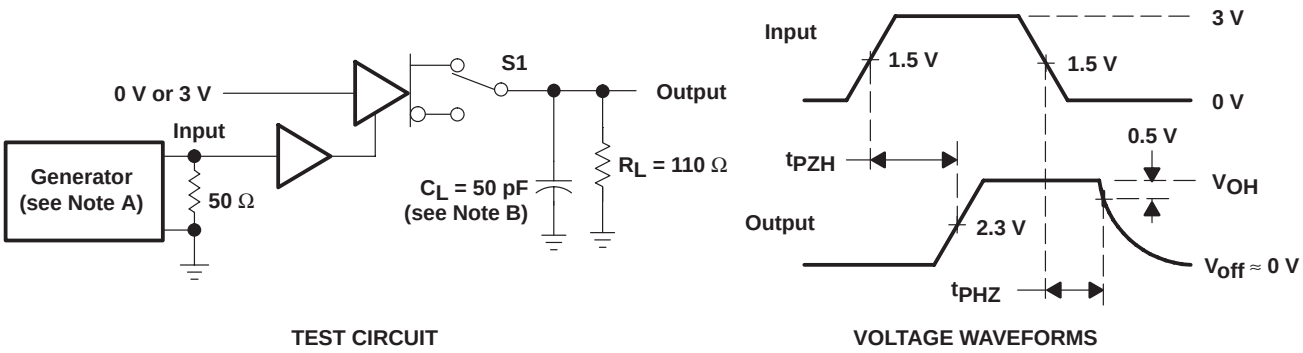
Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

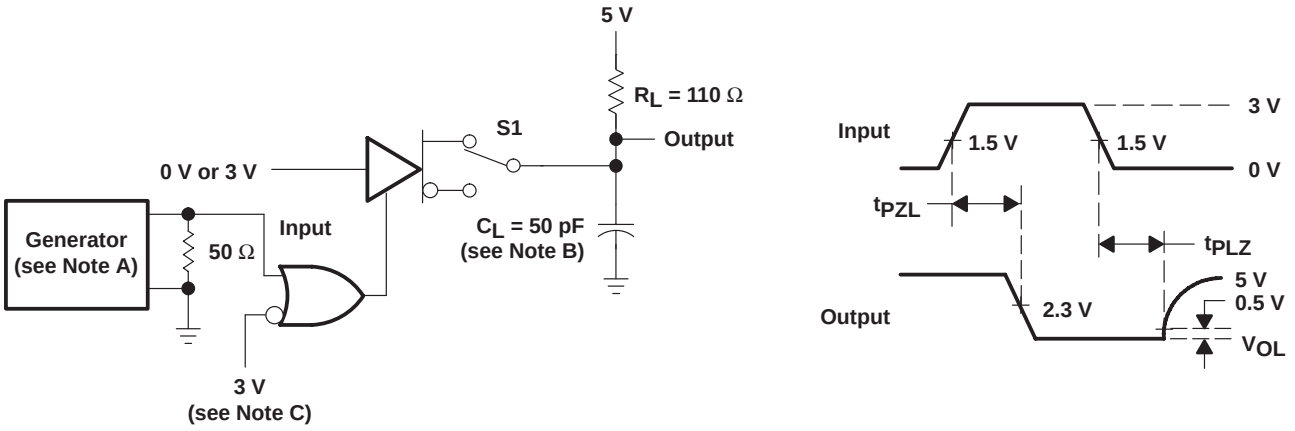
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$..

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

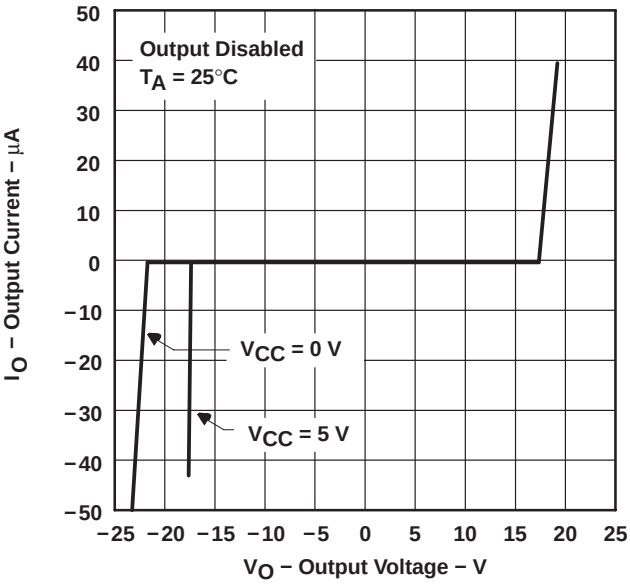


Figure 6

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

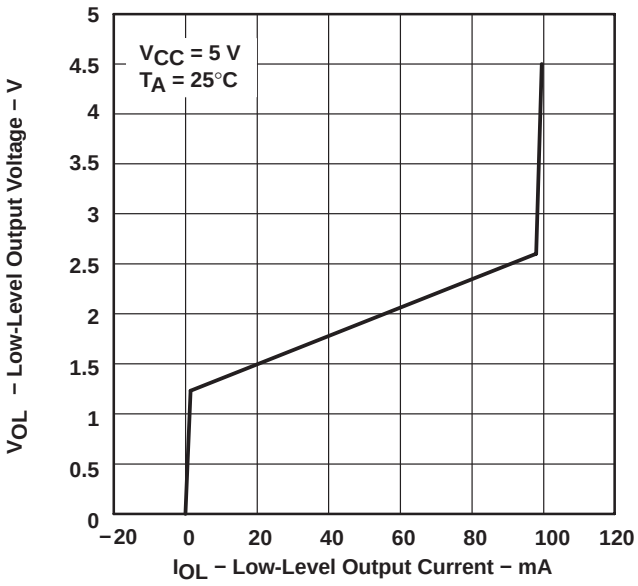


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

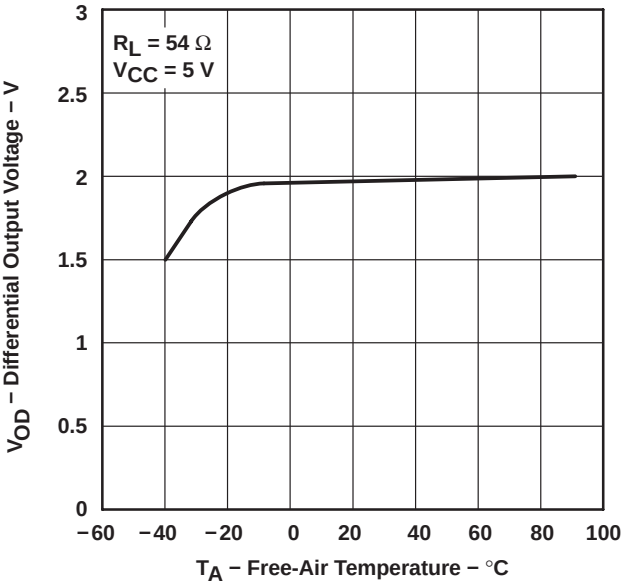


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

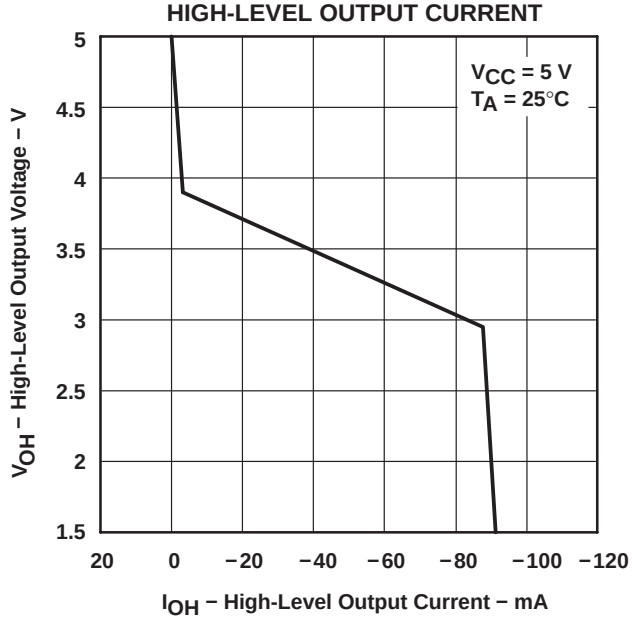


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

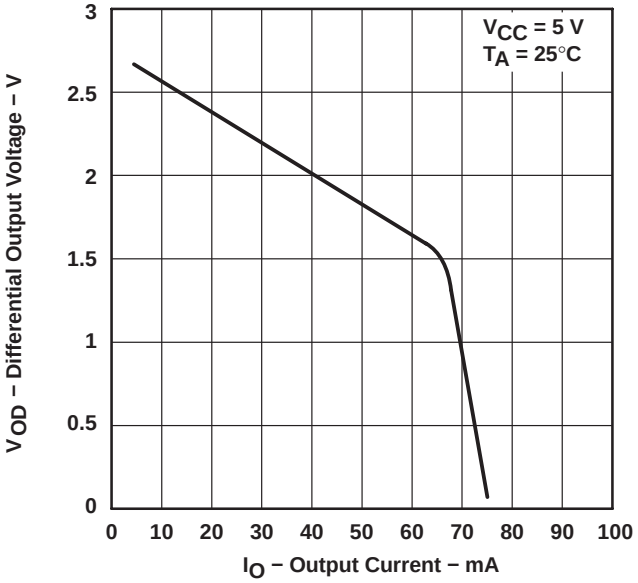


Figure 10

PROPAGATION DELAY TIME, DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

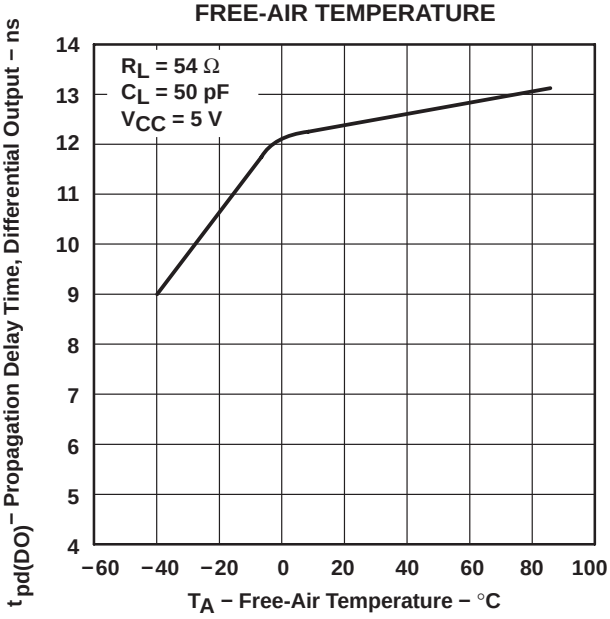


Figure 11

THERMAL CHARACTERISTICS − DW PACKAGE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Junction−to−ambient thermal reisistance, θ_{JA}†	Low-K board, no air flow		96		°C/W
	High-K board, no air flow		62.9		
Junction−to−board thermal reisistance, θ_{JB}	High-K board, no air flow		39.6		
Junction−to−case thermal reisistance, θ_{JC}			29.1		
Average power dissipation, $P_{(AVG)}$	All four channels maximum loading, maximum signaling rate, R_L = 54 Ω, input to D is 10 Mbps 50% duty cycle square wave, V_{CC} = 5.25 V, T_J = 130 °C.			1100	mW
Ambient free−air temperature, T_A	JEDEC high-K board model	−40		85	°C
	JEDEC high-K board model	−40		64	
Thermal shutdown junction temperature, T_{SD}			165		

† See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. $_{\Theta JA}$ is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 12).

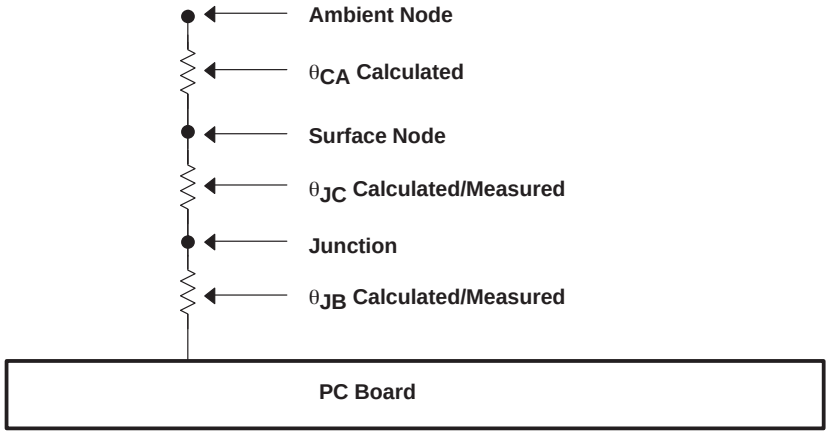
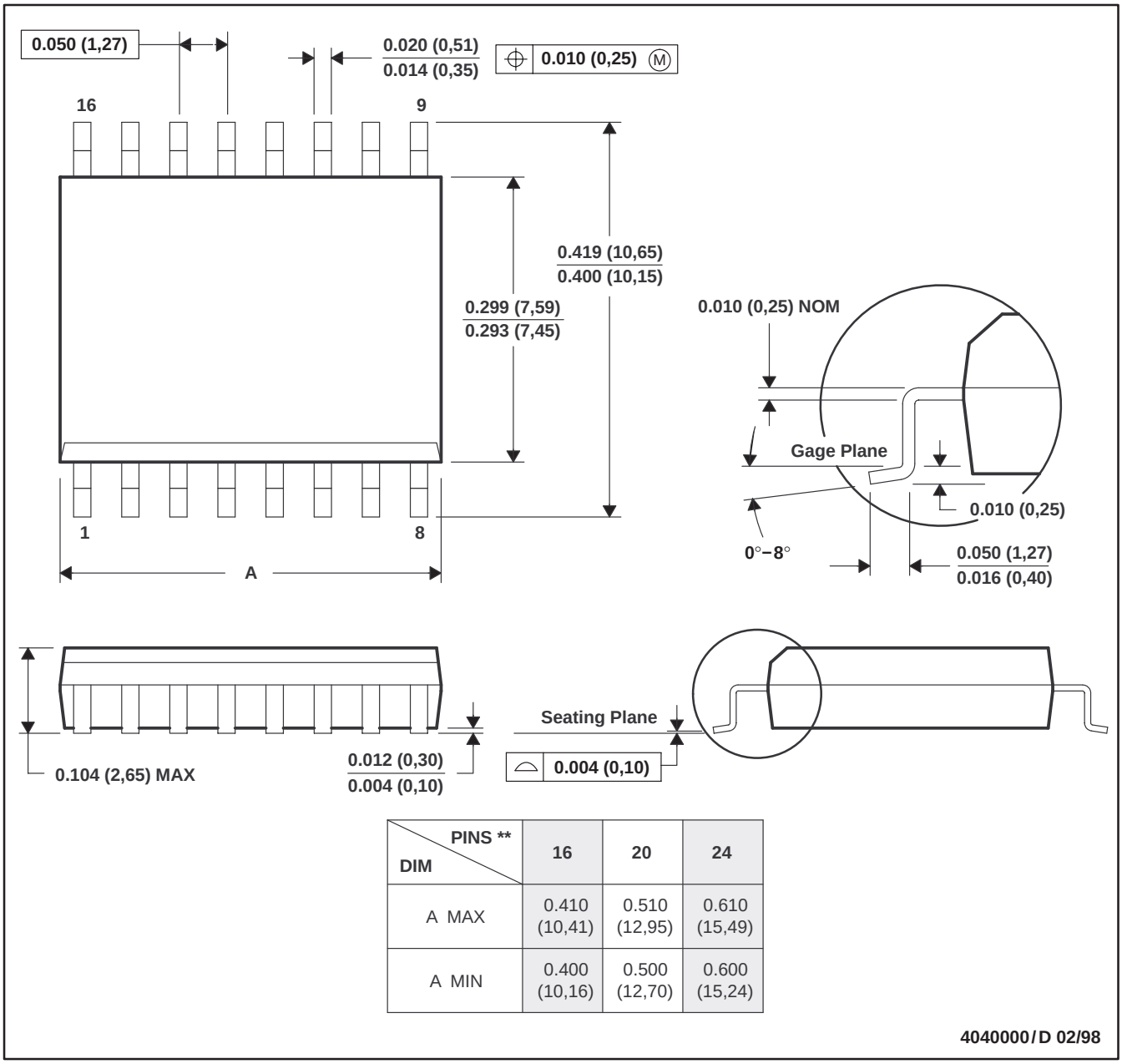


Figure 12. Thermal Resistance

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

4040000/D 02/98

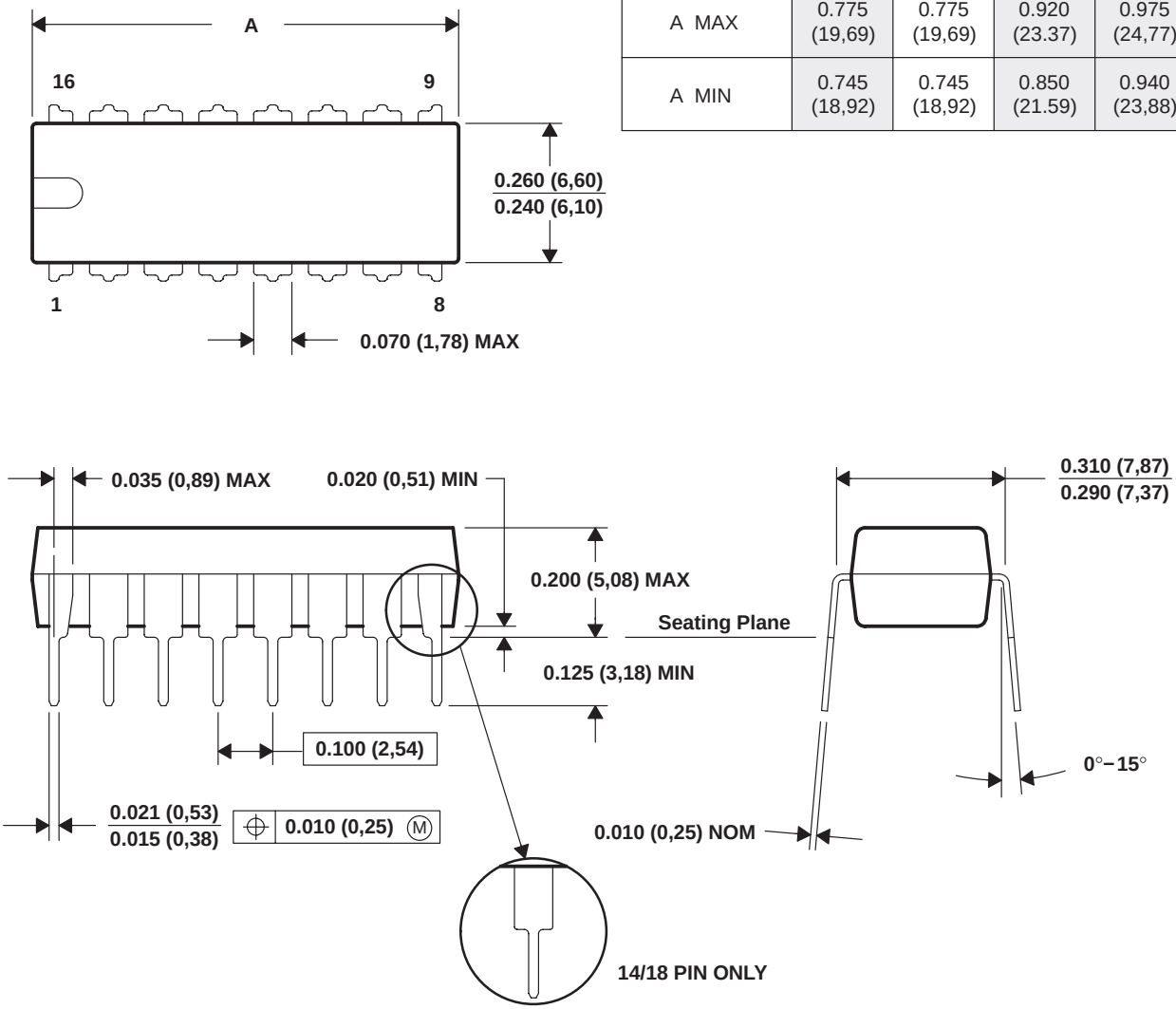
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LBC172DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC172DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN65LBC172NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN75LBC172DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC172DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC172DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC172DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN75LBC172NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN75LBC172 :

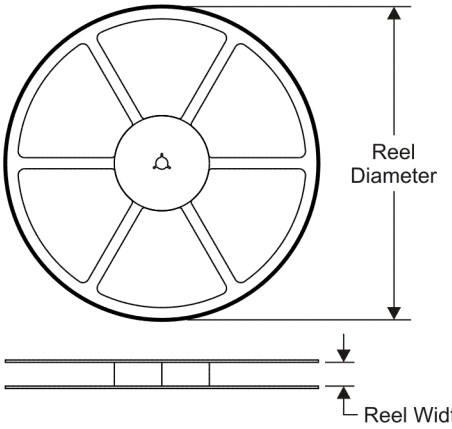
- Military: SN55LBC172

NOTE: Qualified Version Definitions:

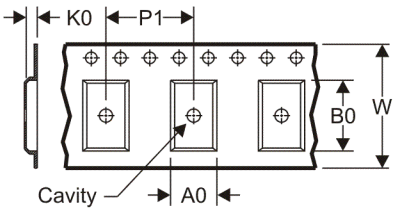
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

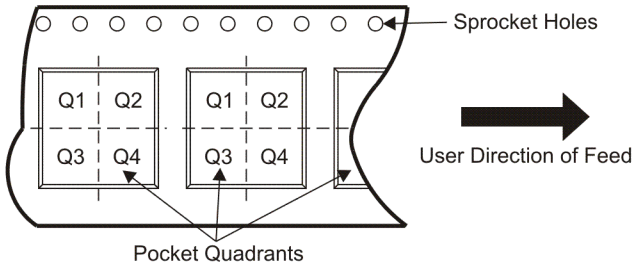


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

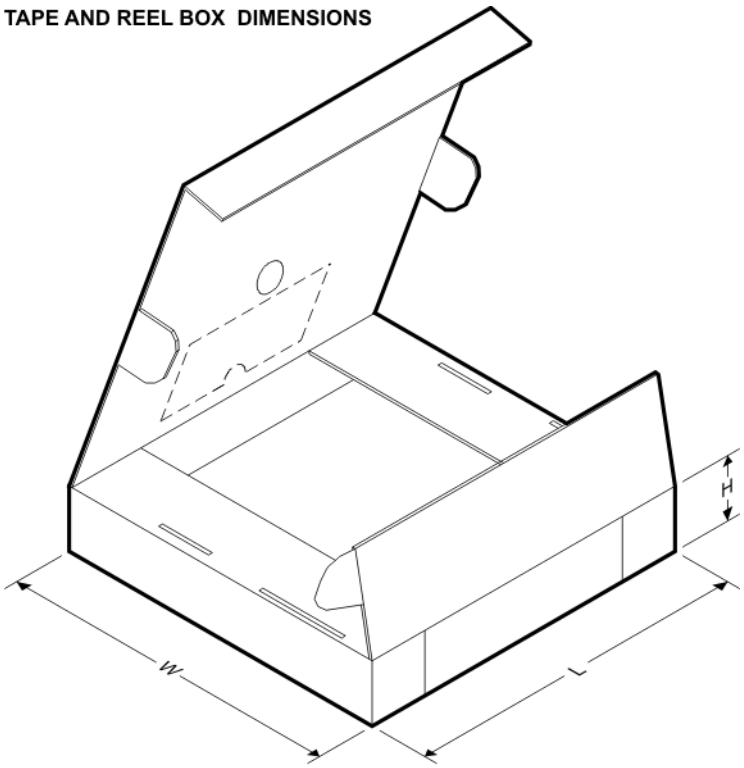
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

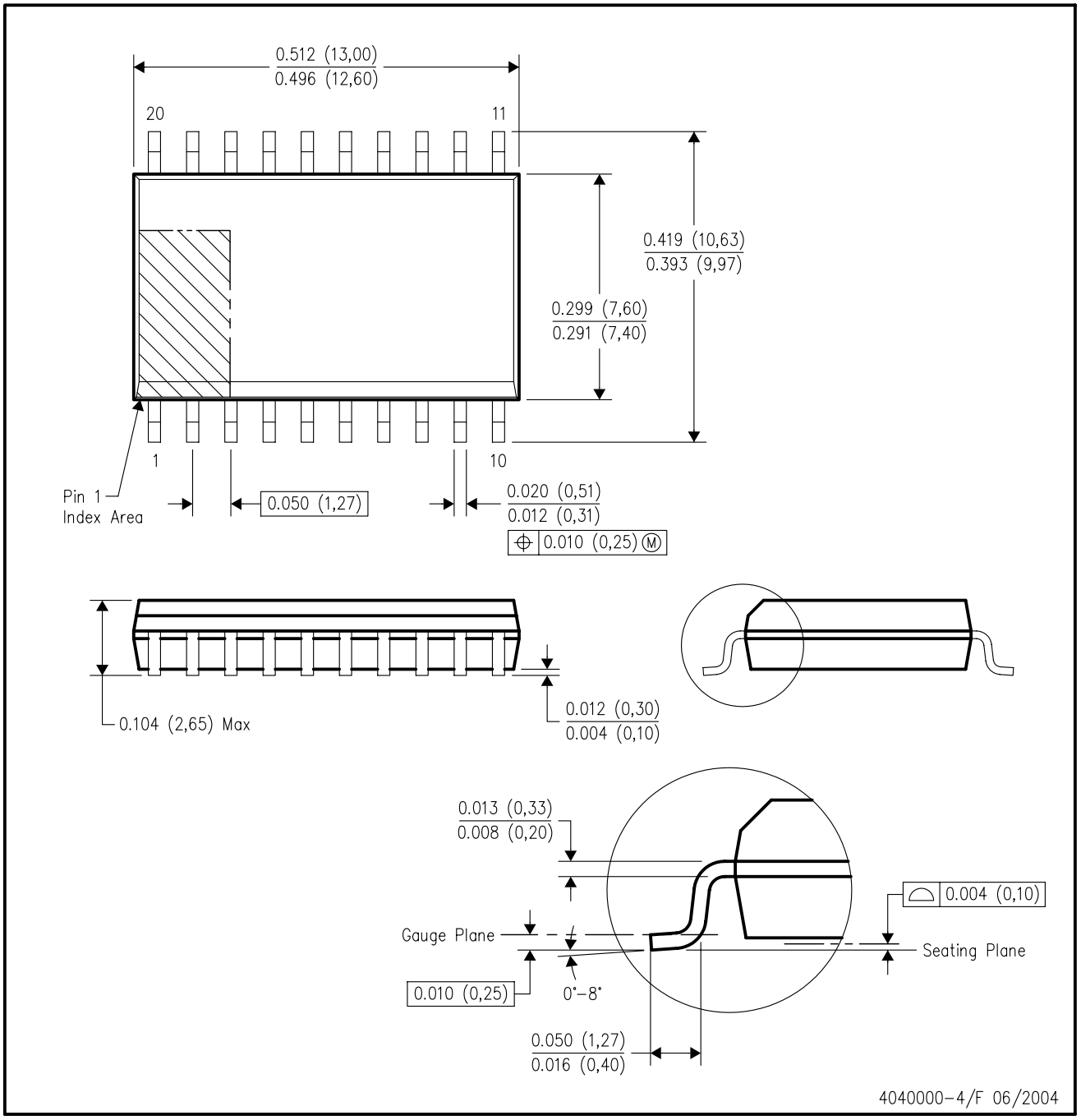
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC172DWR	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

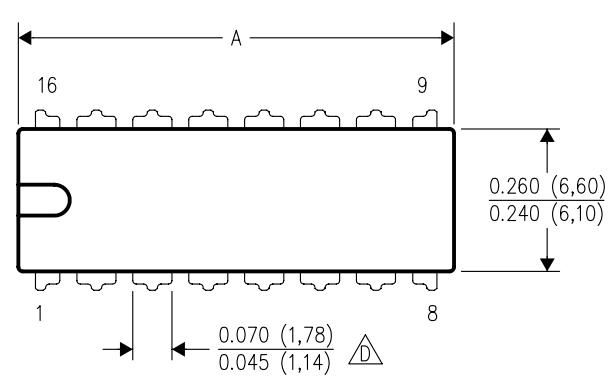


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

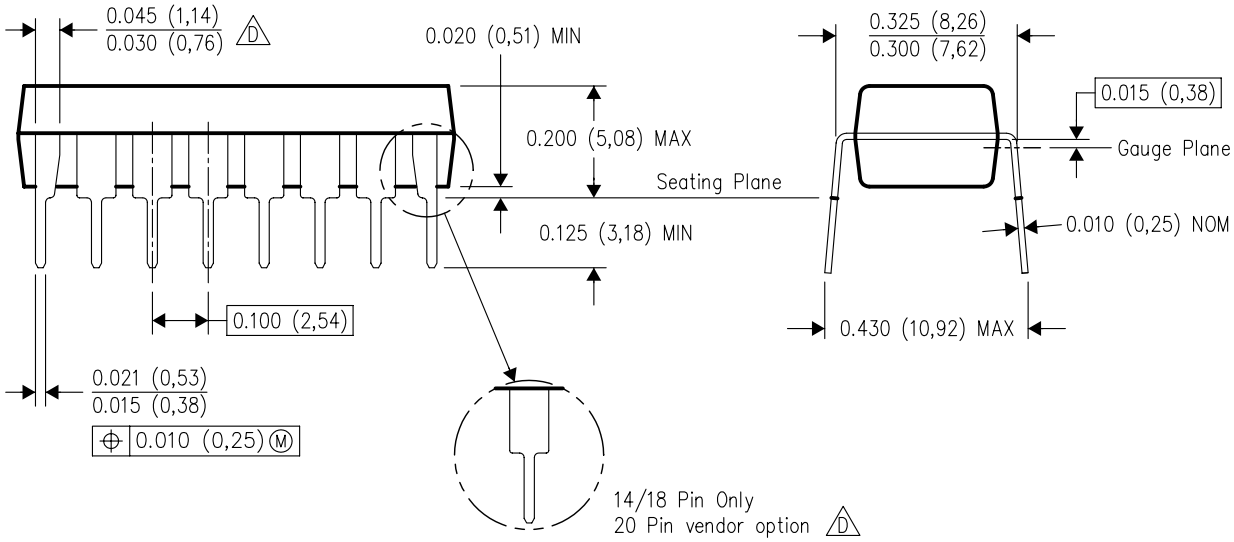
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265